21. (Amended) A graphics accelerator for processing a graphical image, the graphics accelerator comprising:

a texture buffer for storing texture maps and data relating to the texture maps stored in the texture buffer; and

a texture processor that performs texturing operations on the graphical image,

the texture processor including a fetching engine that retrieves texture packets, each texture packet being stored in the texture buffer and being associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer, each texture packet including data relating to the dimensional type of its associated texture map.

35. (Amended) A data structure for storing data relating to a texture map, the texture map having an associated dimension and being stored at a given location in a memory device, the [apparatus] data structure comprising:

a location field identifying the given location in the memory device; and

a dimension field identifying the dimension of the texture map.

REMARKS

Applicant has carefully reviewed and considered the Office Action of September 25, 2001. In the present Amendment, Claims 2 and 23 have been cancelled without prejudice, and Claims 1, 9, 15, 21, and 35 have been amended. Claims 1, 3-22, and 24-38 are pending in the present application Applicant hereby requests entry of this Amendment and Response and further examination of the present application in view of above amendments and following remarks.

In the Office Action mailed on September 25, 2001, claims 1,2, 5-7, 9-13, and 15-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) in view of Tanaka et al. (5,793,376), claims 3, 4, 8, 14, 20-25, and 35-38 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko in view of Tanaka et al and further in view of Priem et al (6,191,794), and claims 26-34 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko and Tanaka et al in view of Priem et al and

further in view of Chimoto (5,550,961). Applicant respectfully traverses this ground of rejection and requests reconsideration thereof in view of the foregoing amendments.

Claim 1

The Office Action rejected claim 1 under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) in view of Tanaka et al. (5,793,376).

Applicant submits that Claim 1, as amended, is not anticipated by Kaneko in view of Tanaka. Amended Claim 1 includes the element wherein each texture data packet is associated with a texture map that is different from texture maps associated with other texture data packets. This limitation is supported by the specification (page 2, lines 17-19; page 8, lines 20-21) and is not disclosed by Kaneko or Tanaka, or a combination thereof.

The Office Action stated that Kaneko discloses the limitation that "each texture packet is associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer," and the Office Action cited the Abstract, Figs. 1-2, Col. 2, Line 35-Col. 4, Line 39, Col. 5, Lines 8-32, Col. 6, Lines 6-56, Col. 11, Lines 27-55, and Col. 11, Lines 57 on, to support that statement.

However, under MPEP §706.02(j), in order to establish a prima facie case of obviousness, the prior art references when combined "much teach or suggest all the claim limitations." Upon review the cited passages, Applicant does not discern where in the cited passages, individually or in combination, the texture packet that is associated with a texture map that is different than the texture maps associated with any other texture packet. Kaneko's Abstract discloses a texture mapping apparatus that applies a texture pattern to an image, and the texture mapping apparatus includes a frame memory, a texture memory, a CPU, a fill address generator, a texture address generator, and a selector. Fig. 1 discloses a block diagram for the texture mapping apparatus, and Fig. 2 discloses a flow chart for the operation of the texture mapping apparatus. Col. 2 line 35-Col. 4 Line 39 seems to disclose a summary of the texture mapping apparatus. Col. 5, Lines 8-32 seem to be a partial description of Fig. 1. Col. 6, Lines 6-56 seem to provide additional description for Fig. 1. Col. 11, Lines 27-55 seem to disclose mapping of texture patterns. And Col. 11, Lines 57 on, only disclose the claims thereof.

Therefore, Applicant respectfully requests the Examiner to clearly explain the cite passages and how they are pertinent to the claimed invention in accord with 37 C.F.R. §1.104 and MPEP §706.02(j). As it stands currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the limitation of Claim 1, as amended, is present, Claim 1, as amended, cannot be rejected as obvious in view thereof.

Claim 3

Claim 3 depends from claim 1. Applicant asserts that claim 3 is allowable over the cited references for the same reason asserted with respect to claim 1.

Applicant notes that Claim 3 further adds an element wherein each texture packet includes data relating to the dimensional type of its associated texture map. The Office Action stated that Kaneko disclosed the same limitation and cited the Abstract, Figs. 1-2, Col. 2, Line 35-Col. 4, Line 39, Col. 5, Lines 8-32, Col. 6, Lines 6-56, Col. 11, Lines 27-55, and Col. 11, lines 57 on, to support this statement, and the Office Action further added that Priem disclosed "the step of determine the change of dimensions in the texture map with respect to the change in the dimensions of pixel in the process of texture mapping." (Col. 8, Lines 5-9, Col. 8, Lines 20-28). The Office Action further stated that there is a motivation for combining Kaneko with Priem "to provide for much faster manipulation of the texture coordinates to obtain texture values and thereby eliminates the need for complicated and expensive circuitry in the graphics accelerator."

Upon review of the cited passages in Kaneko, Applicant does not discern the limitation of claim 3. Therefore, Applicant respectfully requests that the Examiner to clearly explain the cite passages and how they are pertinent to the claimed invention according to 37 C.F.R. §1.104 and MPEP §706.02(j). As it stays currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the limitation of Claim 3 is present, Claim 3 cannot be rejected as obvious in view of such references.

Furthermore, the Office Action has not explicitly shown a suggestion to combine Kaneko with Priem, other than with the guidance of the present application. Applicant asserts there is no suggestion to combine the references in the manner suggested without improper reliance on the present disclosure, and the Office Action has not otherwise pointed to a separate motivational impetus in either of the references. Therefore, the suggested combination cannot be validly used to aggregate elements and arrive at the present invention.

Moreover, the cited passages in Priem seem to disclose a technique for changing dimensions of a texture map, which is different from the limitation of claim 3. Claim 3's limitation concerns including in a texture packet data relating to the dimensional type of an associated texture map and does not concern changing the dimension of a texture map, i.e., claim 3 concerns with data in a texture packet and not with a technique to change dimensions.

Therefore, for the reasons stated above, Applicant submits that claim 3 is patentable over Kaneko in view of Priem.

Claims 4-5

Claims 4-5 depend from claim 1, and Applicant asserts that claims 4-5 are allowable over the cited references for the same reasons asserted with respect to claim 1.

Claims 6-8

Claims 6-8 depend from Claim 1, and Applicant asserts that claims 6-8 are allowable over the cited references for the same reasons asserted with respect to claim 1.

Applicant notes that Claim 6 further adds a limitation of the texture processor including a parsing engine for parsing fetched texture packet and determining information relating to the texture map associated with the fetched texture packet. Claim 7 adds a limitation of the information in claim 6 relates to the location in the texture buffer of the texture map associated with the fetched texture packet. And Claim 8 adds a limitation of the information in claim 6 relates to the number of dimensions of the texture map associated with the fetched texture packet. The Office Action again stated that Kaneko disclosed the same limitations and cited the Abstract, Figs. 1-2, Col. 2, Line 35-

Col. 4, Line 39, Col. 5, Lines 8-32, Col. 6, Lines 6-56, Col. 11 lines 27-55, and Col. 11, Lines 57 on, to support its statement.

Upon review of the cited passages in Kaneko, Applicant does not discern wherein Kaneko the specific limitations of claims 6-8 are located. Therefore, Applicant respectfully requests that the Examiner to clearly explain the cited passages and how they are pertinent to the claimed invention according to 37 C.F.R. §1.104 and MPEP §706.02(j). As it stays currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the limitations of claims 6-8 are present, claims 6-8 cannot be rejected as obvious in view thereof.

Claim 9

The Office Action rejected claim 9 under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) in view of Tanaka et al. (5,793,376).

Claim 9, as amended, is not anticipated by Kaneko in view of Tanaka. Claim 9, as amended, includes a limitation of each texture data packet is associated with a texture map that is different from texture maps associated with other texture data packets. This limitation is supported by the specification (page 2, lines 17-19; page 8, lines 20-21) and is not disclosed by either Kaneko or Tanaka, or a combination thereof.

Therefore, Applicant respectfully asserts that this rejection has been overcome and requests that claim 9 be allowed.

Claims 10-13

Claims 10-13 depend from claim 9, and Applicant asserts that claims 10-13 are allowable over the cited references for the same reasons asserted with respect to claim 9.

Claim 14

Claim 14 depends from Claim 9, and Applicant asserts that claim 14 is allowable over the cited references for the same reasons asserted with respect to claim 9.

Applicant further notes that Claim 14 r adds the element of the texture packet including data relating to the dimensional type of the texture map, the texture map being reconstructed by parsing the texture packet to determine the dimensional type of the texture map, the texture map being reconstructed based upon the determined dimensional type of the texture map. The Office Action stated that Kaneko disclosed the same limitations and cited the Abstract, Figs. 1-2, Col. 2, Line 35-Col. 4, Line 39, Col. 5, Lines 8-32, Col. 6, Lines 6-56, Col. 11, Lines 27-55, and Col. 11, lines 57 on, to support this statement.

Upon review of the cited passages in Kaneko, Applicant does not discern the limitations of claim 14. Therefore, Applicant respectfully requests that the Examiner to clearly explain the cite passages and how they are pertinent to the claimed invention according to 37 C.F.R. §1.104 and MPEP §706.02(j). As it stays currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the limitations of claim 14 is present, claim 14 cannot be rejected as obvious in view thereof.

Claims 15-20

Independent Claim 15, and dependent Claims 16-20cannot be rejected as obvious in view of Kaneko and Tanaka, et al., for the same reasons stated above for the patentability of Claims 9-14.

Claim 21

The Office Action rejected Claim 21 under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) in view of Tanaka et al. (5,793,376) and further in view of Priem et al (6,191,794).

Applicant asserts that Claim 21, as amended, is not anticipated by Kaneko in view of Tanaka and Priem. Claim 21, as amended, includes the element that each texture data packet is associated with a texture map that is different from texture maps associated with other texture data packets. This limitation is supported by the specification (page 2, lines

17-19; page 8, lines 20-21) and is not disclosed by Kaneko, Tanaka, Priem, or their combination.

Furthermore, as stated in the explanation for claim 3, the cited passages in Priem seem to disclose a technique for changing dimensions of a texture map, which is different from "the texture packet including data relating to the dimensional type of its associated texture map." The above limitation in claim 21 concerns including in a texture packet data relating to the dimensional type of an associated texture map and does not concern changing the dimension of a texture map, i.e., the above limitation concerns with data in a texture packet and not with a technique to change dimensions.

Therefore, Applicant respectfully submits that for the above reasons, Claim 21 is allowable over cited references.

Claims 22 and 24

Claims 22 and 24 depend from claim 21, and Applicant asserts that claims 22 and 24 are allowable over the cited references for the same reasons asserted with respect to claim 21.

Claim 25

Dependent Claim 25 is patentable for the same reasons stated above regarding Claim 6.

Claim 26

The Office Action rejected claim 26 under 35 U.S.C. 103(a) as being unpatentable over Kaneko (5,764,237) and Tanaka et al. (5,793,376) and further in view of Priem et al (6,191,794) and Chimoto (5,550,961).

Among the reasons cited, the Office Action stated that Kaneko discloses "locating a second number of consecutive memory locations in the texture memory, the first number being equal to the second number," and the Office Action cited Kaneko's Abstract, Figs. 1-2, Col. 2 , Line 35-Col. 4, Line 39, Col. 5, Lines 8-32.

Upon review of the cited passages in Kaneko, Applicant does not discern the element of Claim 26 as stated above. Therefore, Applicant respectfully requests that the

Examiner to clearly explain the cite passages and how they are pertinent to the above limitation in the claimed invention according to 37 C.F.R. §1.104 and MPEP §706.02(j). As it stays currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the elements of Claim 26 are present, Claim 26 cannot be rejected as obvious in view thereof.

Claims 27-28

Claims 27-28 depends from Claim 26, and Applicant asserts that Claims 27-28 cannot be rejected for the same reasons asserted with respect to the patentability of Claim 26.

Claims 29-31

Claims 29-31 are patentable for the same reasons stated above regarding Claims 26-28.

Claims 32-34

Claims 32-34 are patentable for the same reasons stated above regarding Claims 26-28.

Claim 35

The Office Action rejected claim 35 under 35 U.S.C. 103(a) as being unpatentable over Kaneko in view of Tanaka et al and further in view of Priem et al, and the Office Action cited Kaneko's Abstract, Figs. 1-2, Col. 2, Line 35-Col. 4, Line 39, Col. 5, Lines 8-32, Col. 6, Lines 6-56, Col. 11, Lines 27-55, and Col. 11, lines 57 on, to support this statement..

Upon review of the cited passages, as discussed above for Claim 1, Applicant does not discern where in the cited passages, individually or in combination, a data structure with the specific elements disclosed in Claim 35.

Therefore, Applicant respectfully requests the Examiner to clearly explain the cite passages and how they are pertinent to the claimed invention according to 37 C.F.R.

§1.104 and MPEP §706.02(j). As it stays currently, the Office Action failed to "clearly articulate any rejection [...] so that the applicant has the opportunity to provide evidence of patentability" according to MPEP §706. Without explicit direction as to where in Kaneko the specific elements of Claim 35, as amended, are present, Claim 35, cannot be rejected as obvious in view thereof.

Claims 36-38

Claims 36-38 depend from claim 35, and Applicant asserts that claims 36-38 are allowable over the cited references for the same reasons asserted with respect to claim 35.

Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims 1, 3-22, and 24-38 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (770-291-2125) to facilitate prosecution of this application.

No additional fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees which may be required, including any necessary extensions of time, which are hereby requested, to Deposit Account No. 501403.

Respectfully submitted,

Edwards.
By his Representatives,

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Date 3/22/2022

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 22 day of 03, 2002.

Name

Signature

The process begins at step 400 in which a texture map is retrieved by the host processor 104 (in response to instructions from a drawing or configuration program) from a library of texture maps in a nonvolatile memory. For example, such library may be stored on a hard disk in the computer system 100. The dimension of the texture map then may be determined by the host processor 104 *(e.g.,* by means of a driver application program executed by the host processor 104) and transmitted to the texture processor 302A with the texture map via a message (step 402).

In response to receipt of the texture map, the texture processor 302A responsively converts the texture map into a one dimensional texture map of one or more texture data blocks (step 404). In preferred embodiments, a texture data block ("block") includes data representing a maximum of 512 texels of a texture map.

When converting a two dimensional texture map, each of the blocks of data in the map may be assigned a consecutive sequence number on a block by block basis. This may be completed in any number of ways as known in the art. For example, as shown in figure 5, the top left texture data block may be assigned the first sequence number *(i. e.,* "I "), until the lower right block has the last sequence number (i.e., "20"). Accordingly, each block in figure 5 is identified by a single address number and thus, is converted into a one dimensional map.

If a texture map is a three dimensional texture map, it may be converted into a two dimensional texture map by dividing it into a plurality of two dimensional texture map planes, and then converting each of the two dimensional map planes into one dimensional texture maps as described above. Higher dimensioned texture maps (e.g., four dimensional texture maps) also may be converted into one dimensional texture maps by utilizing the above noted two and three dimensional conversion methods. It should be noted that other methods known in the art may be utilized.

The process then continues to step 406 in which a plurality of consecutive data blocks in the texture memory 304A are located. The process preferably is done via software executing on the texture processor 302A. Of course, the located data blocks must equal at least the number of

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resultant data blocks of the converted texture map. For example, at least twenty data consecutive data locations must be located in the texture memory 304A for storing the texture map shown in figure 5.

Once the appropriate data blocks are located, the process continues to step 408 in which the converted one dimensional texture maps are stored in the located data locations (i.e., the appropriate blocks) in the texture memory 304A. In preferred embodiments, the texture processor 302A is configured via hardware to store the converted texture map in the texture memory 304A. A texture packet (discussed below and shown in figure 7) then is created at step 410 and stored in the texture memory 304A. In preferred embodiments, the location of the texture packet is stored in a packet look-up table that is utilized by the fetching engine 308 to retrieve such packet. Details of the packet retrieval process are discussed below.

Among other data, the texture packet may include the location of the stored converted texture map in the texture memory 304A, and the dimensional size of the texture map prior to being converted. For example, a texture packet may contain data indicating that the texture map shown in figure 5 is twenty data blocks long and stored in memory locations 1-20 in the texture memory 304A. Each texture packet in texture memory 304A preferably has a single unique texture map associated with it, and is stored in texture memory 304A in a location that is preconfigured to store texture packets. In some embodiments, the single texture map may include a family of mipmaps (discussed below).

It should be noted that the steps of the process shown in figure 4 may be preformed in orders other than that shown in the figure. For example, some steps may be performed simultaneously, while other steps may be performed either before or after each other.

Accordingly, this process enables the texture memory to store texture maps of different dimensions. For example, preferred embodiments of a given texture memory 304A can store texture data for one, two, three and four dimensional texture maps. To that end, the texture memory 304A preferably is logically structured as two banks of linear arrays of memory blocks. Each memory block has a size that corresponds to the size of the texture

I claim:

1. A graphics accelerator for processing a graphical image, the graphics accelerator comprising:

a texture buffer for storing texture maps and data relating to the texture maps stored in the texture buffer; and

a texture processor that performs texturing operations on the graphical image,

the texture processor including a fetching engine that retrieves texture packets, each texture packet being stored in the texture buffer and being associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer, each texture packet including data relating to the location of its associated texture map in the texture buffer.

3. The graphics accelerator as defined by claim 1 wherein each texture packet includes data relating to the dimensional type of its associated texture map.

4. The graphics accelerator as defined by claim 3 wherein the dimensional type of each texture map is one of a one dimensional texture map, a two dimensional texture map, and a three dimensional texture map.

5. The graphics accelerator as defined by claim 1 wherein the texture processor further includes:

an input for receiving a texture message indicating that a texture map is to be utilized by the texture processor, the fetching engine responsively retrieving selected texture packets from the

texture buffer in response to receipt of the texture message.

6. The graphics accelerator as defined by claim 5 wherein the texture processor further includes:

a parsing engine for parsing a fetched texture packet and determining information relating to the texture map associated with the fetched texture packet.

7. The graphics accelerator as defined by claim 6 wherein the information relates to the location in the texture buffer of the texture map associated with the fetched texture packet.

8. The graphics accelerator as defined by claim 6 wherein the information relates to the number of dimensions of the texture map associated with the fetched texture packet.

9. A method of applying texture to a graphical image, the method comprising:

locating a texture packet identifying the location of a texture map in a memory device, wherein the texture packet is associated with the texture map that is different than texture maps associated with other texture packets;

parsing the texture packet to determine the location of the texture map;

retrieving, based upon the determined location, the texture map from the memory device; and

applying the texture map to the graphical image.

10. The method as defined by claim 9 wherein the texture packet is located by accessing a record identifying the location of the texture packet.

11. The method as defined by claim 9 wherein the memory device is texture memory.

12. The method as defined by claim 9 wherein the texture packet is stored in the memory device

13. The method as defined by claim 9 further comprising

reconstructing the texture map after it is retrieved from the memory device.

14. The method as defined by claim 13 wherein the texture packet includes data relating to the dimensional type of the texture map, the texture map being reconstructed by parsing the texture packet to determine the dimensional type of the texture map, the texture map being reconstructed based upon the determined dimensional type of the texture map.

15. A computer program product for use on a computer system for applying texture to a graphical image, the computer program product comprising a computer usable medium having computer readable program code thereon, the computer readable program code including:

program code for locating a texture packet identifying the location of a texture map in a memory device, wherein the texture packet is associated with the texture map that is different than texture maps associated with other texture packets;

program code for parsing the texture packet to determine the location of the texture map;

program code for retrieving, based upon the determined location, the texture map from the memory device; and

program code for applying the texture map to the graphical image.

16. The computer program product as defined by claim 15 wherein the program code for locating includes program code for accessing a record identifying the location of the texture packet.

17. The computer program product as defined by claim 15 wherein the memory device is texture memory.

18. The computer program product as defined by claim 15 wherein the texture packet is stored in the memory device

19. The computer program product as defined by claim 15 further comprising:

program code for reconstructing the texture map after it is retrieved from the memory device.

20. The computer program product as defined by claim 19 wherein the texture packet includes data relating to the dimensional type of the texture map, the program code for reconstructing comprising

program code for parsing the texture packet to determine the dimensional type of the texture map, the texture map being reconstructed based upon the determined dimensional type of the texture map

21. (Amended) A graphics accelerator for processing a graphical image, the graphics accelerator comprising:

a texture buffer for storing texture maps and data relating to the texture maps stored in the texture buffer; and

a texture processor that performs texturing operations on the graphical image,

the texture processor including a fetching engine that retrieves texture packets, each texture packet being stored in the texture buffer and being associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer, each texture packet including data relating to the dimensional type of its associated texture map.

22. The graphics accelerator as defined by claim 21 wherein each texture packet includes data relating to the location of its associated texture map in the texture buffer.

linear texture memory of a graphics accelerator, the computer program product comprising a computer usable medium having computer readable program code thereon, the computer readable program code including

program code for determining the dimension of the texture map;

program code for converting the texture map to a one dimensional texture map if the dimension of the texture map is determined to be more than one dimensional, the one dimensional texture map having a first number of consecutive data blocks;

program code for locating a second number of consecutive memory locations in the texture memory, the first number being equal to the second number; an

program code for storing the one dimensional texture map in the located memory locations in the texture memory.

33. The computer program product as defined by claim 32 wherein the texture map is two dimensional, the program code for converting comprising:

program code for defining a plurality of data blocks within the texture map; and

program code for assigning a sequence number to each of the data blocks, the sequence numbers being consecutive numbers.

34. The computer program product as defined by claim 32 wherein the program code for storing comprises

program code for consecutively storing each consecutive data block of the one dimensional texture map in the located memory locations.

35. A data structure for storing data relating to a texture map, the texture map having an associated dimension and being stored at a given location in a memory device, the data structure comprising

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a location field identifying the given location in the memory device; and